



V-Series: The Image Processing

Deploying individual features and reducing host CPU load by user programmable framegrabbers

In contrary to visual documentation purposes, most applications in Machine Vision require an image processing. The content of each image is processed on its informational value. It is reduced on a numerical value or a qualitative statement. For this purpose, the image is processed by various levels of an image analysis.

The first step of a processing chain is a thresholding, followed by edge detection and an addition of pixels in a defined area, for example. Each level requires computation time, which determines the overall latency of an application in total.

The V-series frame grabbers of Silicon Software support an image acquisition as well as an on-board image processing. For this purpose, interfaces to the graphical programming environment VisualApplets have been implemented on the frame grabber and the hardware resources have been extended. The implementation allows that FPGA feature sets, so-called hardware applets with individual functions can be loaded and run on the frame grabber. Additionally the V-series is prepared to run SmartApplets, which covers application related image processing libraries. SmartApplets libraries are available as high-quality image processing for thresholding, object segmentation and classification and 3D measurement.

Silicon Software has developed software tools that allow programmers to implement individual functions on FPGA hardware. VisualApplets is aimed at hardware programmers as well as software engineers to realize image processing applications in Machine Vision. The software environment can be used to program a simple filter operation, complex image processing algorithms or even complete vision application in hardware.

The use of FPGAs in Machine Vision is very versatile. Typical applications cover all types of filtering operations, time-consuming image binarization or image addition. Programming of individual trigger functions and signal processing are also important features in applications. But even complex image processing such as 3D laser triangulation, compressions, a blob analysis for object segmentation and tracking can be implemented and provide an image pre-analysis, which allows the software-based image processing to complete the final analysis even with a high amount of image data in a shorter time with less CPU power.

To use a variety of functions, function specific hardware applets can be synthesized that can be loaded in milliseconds and are immediately ready for use. Alternatively, a complex design can be synthesized, which can process different algorithms and parameters.

By the parameterization of a VisualApplets design, FPGA registers are defined, which represent the interfaces to the application software. Parameter values can be changed during runtime by software accesses from the application.



microEnable IV AD1-mPoCL

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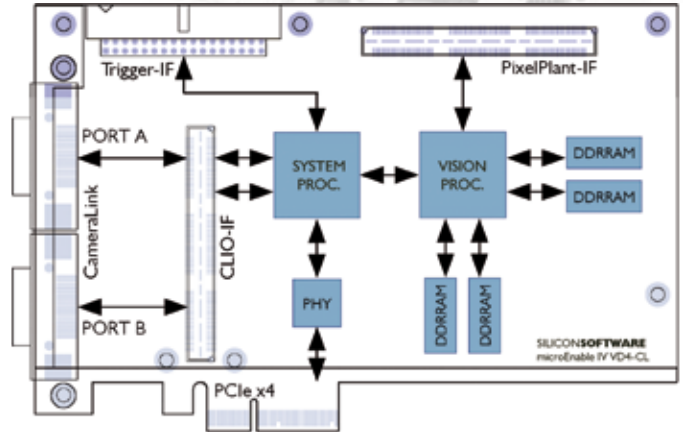




By reload of hardware applets and a re-configuration by a register access, FPGA programming is a highly flexible and powerful image processing solution.



The FPGA is designed for high parallelism and high data rates. Even simple preprocessing will amortized the use of FPGAs. By outsourcing of image processing tasks on the frame grabber, the CPU is unloaded from compute-intensive calculations. This allows building systems with low performance CPUs and generates less heat.

There are three models available for Camera Link standard and two models available for GigE Vision standard. microEnable IV VD1-CL support Camera Link cameras with 10 taps FULL configuration and a bandwidth of 800 MBytes/s, but only provides an PCI Express x1 interface to the PC with 220 MBytes/s. By data reducing image processing, the frame grabber provides a lossless analysis result in real-time. The Camera Link frame grabbers microEnable IV VD4-CL and VD4-PoCL are based on an x4 PCI Express interface and cover the DMA900 technology. Hereby a data transfer to the host PC of 850 MBytes/s is supported. This allows a data transfer of the original image and of additional information and results. For both of the standards Camera Link and GigE Vision, „power over“ models are available.



Schematic layout of microEnable IV VD4-CL

Available or planned models:

Standard / Frame Grabber	Description
V-Series for Camera Link	
microEnable IV VD1-CL	2-channels image processing board
microEnable IV VD4-CL	2-channels high-performance image processing board
microEnable IV VD4-PoCL	2-channels high-performance image processing board with power supply for cameras PoCL
V-Series for GigE Vision	
microEnable IV VQ4-GE	4-channels image processing board
microEnable IV VQ4-GPoE	4-channels image processing board with voltage injector (optional)

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